Commercial Spread-Spectrum MMIC Power Amplifiers

Single chip, MMIC power amplifiers for 2.4 and 5.8 GHz commercial spread-spectrum applications are described with measure only 3.0 x 1.7 mm.

Tom Apel
Ratan Bhatia
Teledyne Microwave
Mountain View, California

GaAs MMIC technology offers superior gain per stage and better multistage power added efficiency, when compared to applications in which Silicon is used above L-Band. Even at L-Band GaAs has appropriate uses. The chips discussed here provide very affordable solutions to the need for general purpose power amplifiers in unlicensed commercial spread-spectrum transceivers [1].

The FCC authorized 902-928, 2400-2483 and 5725-5850 MHz for spread spectrum communications.

These MMICs provide a repeatable and cost effective alternative to conventional hybrid and discrete power amplifiers. Bias circuitry is integrated so assembly time and cost are lower. Tuning is eliminated. Power and efficiency performance is quite satisfactory, with useful gains in excess of 20 dB and 1 dB compression power output of 0.5 watts. This performance was obtained on a first pass through design, fabrication and test, with an overall cycle time of 2.5 months.

The FCC authorized frequency bands for spread-spectrum systems are 902 to 928 MHz, 2400 to 2483 MHz. and 5725 to 5850 MHz. The requirements for transmitter power output are +30 dBm EIRP with spread-spectrum modulation.

With typical antenna gains in 0 to 3 dBi range, the maximum power output required from the power amplifier (PA) is + 27 to +30 dBm. The two PAs described herein are designed to provide power output capability greater than +27 dBm at 1dB gain compression from a +5 V drain supply.

Circuit Design

Based on the requirements of an existing direct-sequence spread-spectrum system, the following minimum design goals were established for the 2.4 and 5.8 GHz. power amplifiers:

Frequency Band	2.45 GHz +/-50 MHz	5.8 GHz +/-75 MHz
Gain	25 dB	20 dB
Power Output @ 1dB GC	+27 dBm	+27 dBm
Power Added Efficiency	20%	20%
Input VSWR	2:1	2:1
Output Third Order Intercept	35 dBm	35 dBm
Operating Temperature Range	0 to +70 C	0 to +70 C

The power amplifier load-line designs were based on nominal +5v operation. For improved efficiency, FETs are biased in Class-AB. The output network of the final amplifier provides second harmonic tuning, also for efficiency improvement.

The power amplifiers' output network is also tuned for second harmonic to enhance Class AB efficiency.

Optimum power loading for this low voltage application and FET process was obtained by matching an equivalent source admittance of 47.6+j5.9 mS per mm of gate-width, at 2.45 GHz. In support of these designs, load-pull data was gathered from 300 and 600 micron devices with an automated tuner system manufactured by Focus Microwaves. Test conditions were Vds= +5v and various degrees of Class-AB bias which ranged from 20% Idss to 50% Idss quiescent current.

Circuit simulation was performed in both linear and non-linear forms. Non- linear simulation used the Curtice-Cubic FET large-signal model in a harmonic balance type simulator. Modeled device power and efficiency were both within 1dB of measured levels.

A final amplifier stage gate-width (Wg) of 3.0 mm was selected, based on power and efficiency requirements. For high efficiency, FET Wg ratio's between final and driver stages was set as high as 7 dB. The Wg ratio between predriver and driver stages was less aggressively set at 3 dB, due to impedance level and gm considerations. The resultant driver and predriver gate-widths are 600 and 300 microns, in the 2.4 GHz PA, respectively. The 5.8 GHz PA's respective gate- widths are 720 and 300 microns.

Gate interface networks are lossy to aid stability, bandwidth and bias supply. The amplifiers are unconditionally stable.

Gate interface networks were lossy loaded for stability, bandwidth and bias feed considerations. Drain matching network topologies were selected based on bias considerations as well as RF impedance match. Gate bias distribution on chip is de-Qed and decoupled by series resistors in each line. The drain bias feeding structure is shunt loaded with a series RC damper. Additional drain isolation is provided by series resistors to the first two stages. The small voltage drop incurred there is tolerable and has been budgeted into the design. The chip is unconditionally stable. Schematic diagrams of the two PA designs are shown in Figure 1 and 2.

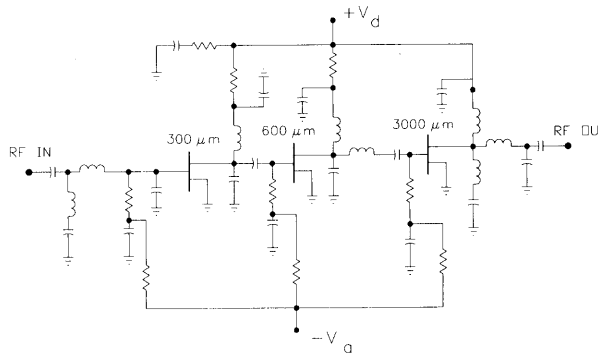

Figure 1. 2.4 GHz MMIC PA RF schematic.

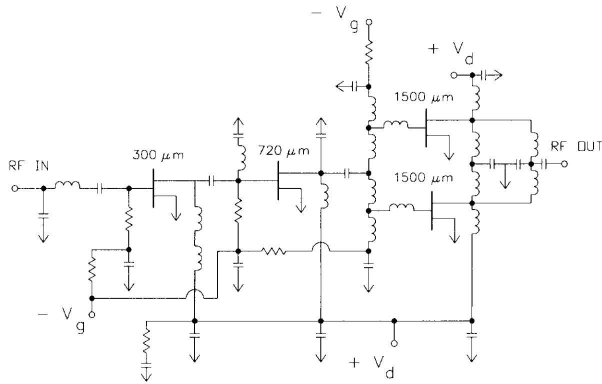

Figure 2. 5.8 GHz MMIC PA RF schematic.

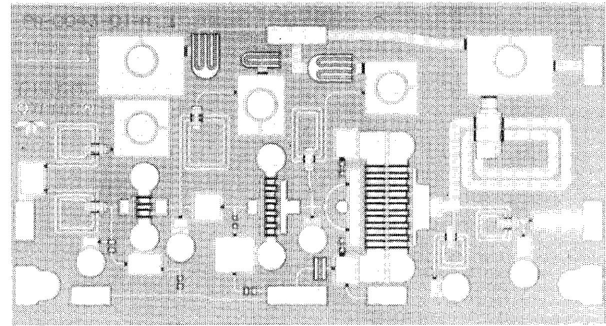

Figure 3. 2.4 GHz MMIC power amplifier.

Fabrication

The active devices are supported by a standard 0.5 micron GaAs MESFET MMIC ion implanted foundry process. Gates are written with E-beam lithography and realized in a double recess. The process includes Silicon Nitride MIM capacitors, Tantalum Nitride and GaAs resistors, and low-loss transmission line elements. Low inductive grounding paths are provided through 50 micron diameter via holes. Typical DC parameters for a 1 mm device are Vb = +15v, Idss = 320mA, Vp = - 3.5v, Gm = 135mS. Chip area is conserved by distributing bypass MIM capacitors around via pads. This technique has been previously described in [2].

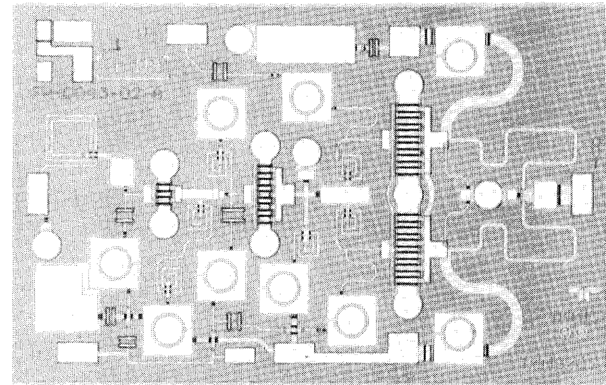

Figure 4. 5.8 GHz MMIC power amplifier.

Measured Results

All of the design specifications were met with the first MMIC pass.

The first-pass results on these MMICs met all the design specifications. A photo of the MMICs is shown in Figures 3 and 4. The chip size of the 2.4 GHz MMIC is 3.0 x 1.7 x 0.1 mm and that of the 5.8 GHz. MMIC is 3.0 x 1.9 x 0.1 mm. Measured data has been taken with the devices mounted in a low-cost surface- mount package. The only external components required are two external bypass capacitors in the positive and negative bias paths for additional out of band decoupling, to ensure against bias path induced low frequency oscillations. The packaged chip assemblies are shown in Figure 5 and Figure 6.

The measured gain and return loss for the two MMICs are shown in Figures 7 and 8. Clearly, the 2.4 GHz PA has typical small-signal gain of 28 to 30 dB and input return loss below -10 dB over most of

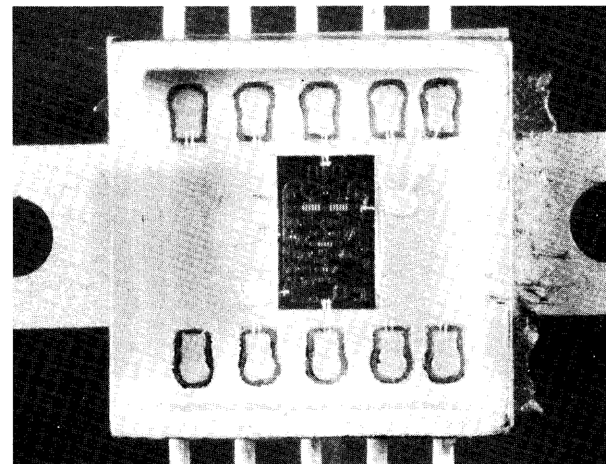

Figure 5. 2.4 GHz packaged MMIC power amplifier.

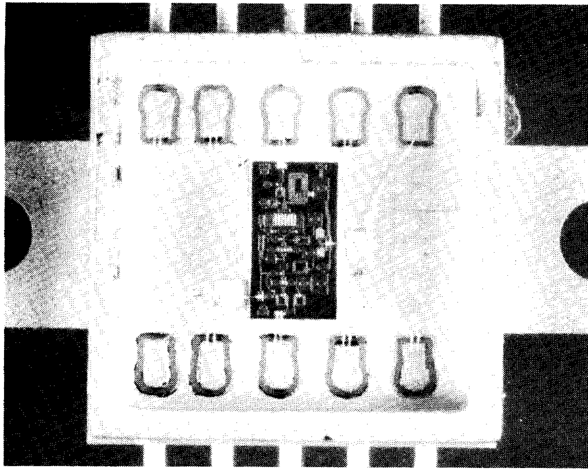

Figure 6. 5.8 GHz packaged MMIC power amplifier.

the operating band. The 5.8 GHz PA provides a typical gain of 23 dB with less than -12 dB of input return loss over it's operating band. Small-signal test conditions are T = 25 degrees C and a bias of +5v, 410 mA.

The 2.4 GHz chip has power output greater than 1 watt and 32% added efficiency.

The measured output power and efficiency of the 2.4 GHz chip is displayed in Figures 9 through 12.

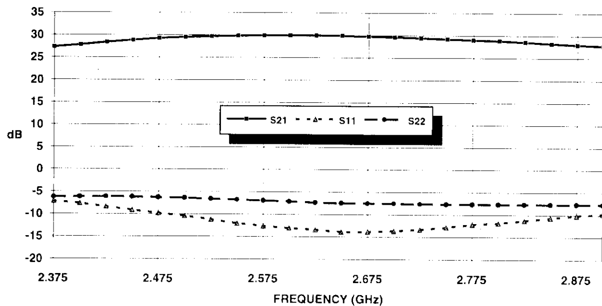

Figure 7. 2.4 GHz MMIC PA small-signal performance.

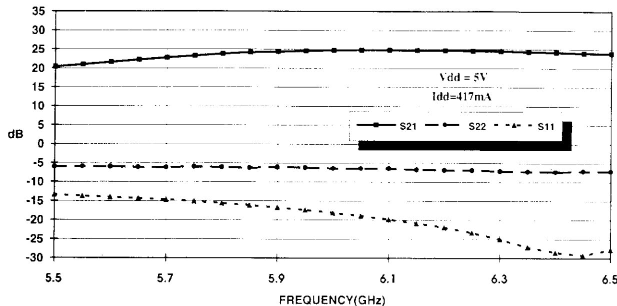

Figure 8. 5.8 GHz MMIC PA small-signal performance.

Figure 9 shows the -1 dB compression power versus frequency for a 35% Idss bias. The -1 dB compressed power performance trade-off with operating point (drain voltage and quiescent current) is illustrated in Figure 10. Similarly, the efficiency impact of operating point is shown in Figure 11. It can be seen that power output greater than 1 watt and associated power added efficiency above 32% has been typically achieved from this MMIC.

Power and efficiency at Vds = +5v are typically +28 dBm and 25%, respectively. Since a primary application for this chip is direct sequence spread-spectrum modulated signals, Figure 12 has been included to illustrate the operating point effect on spectral regrowth of the second (5th order) side-lobe. The power level displayed is associated with a 3 dB degradation in the second (5th order) side-lobes. Typical 3rd order output intercept point for the 2.4 GHz PA at 2.45 GHz is about 36 dBm at Vds = +5V.

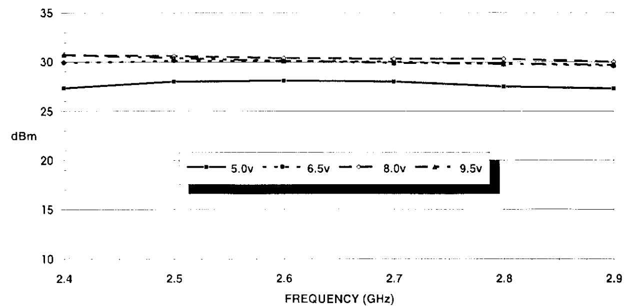

Figure 9. 2.4 GHz MMIC PA -1 dB compression power.

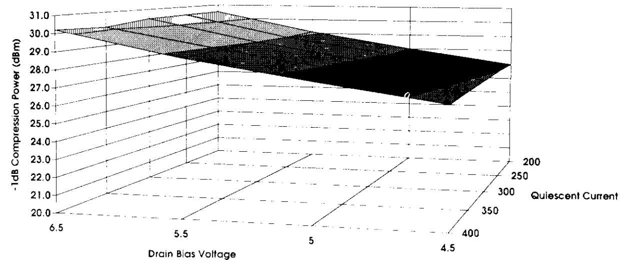

Figure 10. 2.4 GHz MMIC PA -1dB compression power.

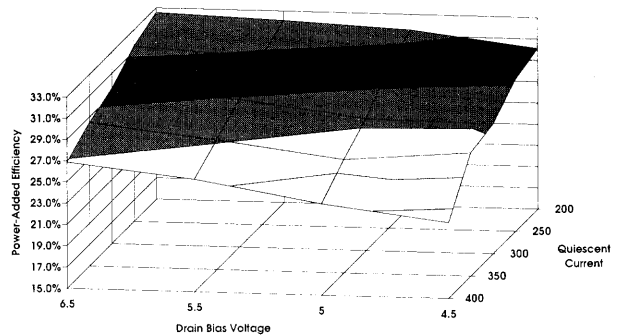

Figure 11. 2.4 GHz MMIC PA efficiency at -1dB compression.

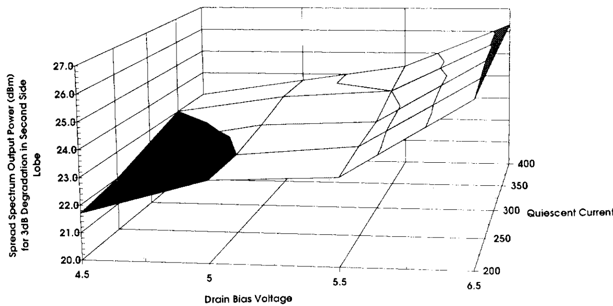

Figure 12. 2.4 GHz MMIC PA spread spectrum output power.

The 5.8 GHz chip delivers up to 1 watt and 20% added efficiency at appropriate bias levels.

The power and efficiency performance of the 5.8 GHz chip is shown in Figures 13 and 14. This chip delivers a minimum output power of 26 dBm with associated power-added efficiency of 18%. At appropriate bias levels, 1 watt power levels and associated power added efficiencies above 20% are typically measured. The third order output intercept point at 5.85 GHz is typically 35 dBm at Vds = +5v.

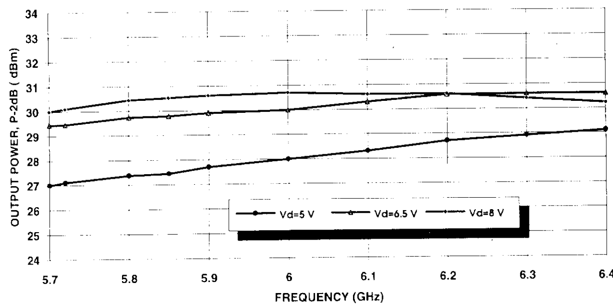

Figure 13. 5.8 GHz MMIC PA output power(P-2dB) vs frequency and bias voltage.

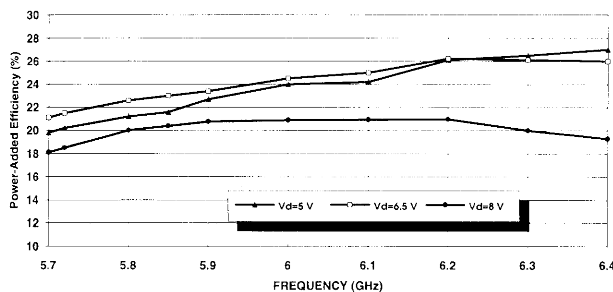

Figure 14. 5.8 GHz MMIC PA power-added efficiency @ P-2dB vs frequency and bias voltage.

Acknowledgments

The authors wish to acknowledge the encouragement and support extended by Dr. Steve Ludvik of Teledyne Microwave. We are also grateful to Dr. H. Sun for help with non-linear analysis and Eric Creviston for assistance in characterizing the amplifiers.

References

1. A. Ward, "Survey of Component Technologies for 900, 2400, and 5700 MHz Unlicensed Spread Spectrum Transceivers," RF Expo-West Proceedings, pp197-208, March 1992.
2. T. Apel and S. Ludvik, "A Compact, High Gain, 2-20 GHz MMIC Amplifier," 1992 IEEE Journal of Solid State Circuits, Vol.27, No.10, pp.1463-1469, Oct.1992.

Thomas Apel *received BS degrees in Physics and Mathematics from Loras College and MSEE from the University of Wisconsin (Madison) in 1976 and 1978, respectively. In 1989 he joined Teledyne Monolithic Microwave as a Senior Member of Technical Staff. He is actively engaged in GaAs MMIC circuit development for commercial and defense sector applications. Prior to joining Teledyne, he held positions with Avantek, and Hughes (Torrance Research Center) as Power Amplifier Product Line Engineering Manager and Section Head for Power Components, respectively. Mr. Apel holds four Patents and is a member of the IEEE.*

Ratan Bhatia received his BSEE from Birla Institute of Technology & Science and MSEE from Arizona State University in 1982 and 1984, respectively. Since 1988, he has been employed at Teledyne Microwave as a member of technical staff. His primary work is in the area of GaAs MMIC circuit development. Circuit designs worked on include LNAs, Power Amplifiers, Up/Downconverters and VCOs for commercial and military applications. Prior to joining Teledyne, he was at Litton Solid State, engaged in GaAs MMIC development. He also worked at Avantek, Inc., from 1984 to 1986 as a design engineer developing MMIC LNAs and medium power amplifiers. Mr. Bhatia is a member of IEEE.